Available online at www.sciencedirect.com
SCIENCE DIRECT
ELSEVIER
Polymer 46 (2005) 563–568
polymer
www.elsevier.com/locate/polymer

The effects of the temperature on the some parameters obtained from current–voltage and capacitance–voltage characteristics of polypyrrole/*n*-Si structure

Ş. Aydoğan*, M. Sağlam, A. Türüt

Department of Physics, Faculty of Sciences and Arts, University of Atatürk, 25240 Erzurum, Turkey

Received 8 September 2004; received in revised form 4 November 2004; accepted 4 November 2004
Available online 30 November 2004

Abstract

The polypyrrole/*n*-Si structure has been directly formed onto the *n*-Si substrate by the electrochemical polimerization of the organic polypyrrole at 45 °C electrolyte temperature. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of the structure have been determined at various temperatures in the range of 77–300 K and different frequencies. Some diode parameters have been calculated from these curves. It has been seen that the measured capacitance decreases with increasing frequency due to a continuous distribution of the interface states in the frequency range of 10 kHz–1 MHz. The barrier heights values obtained from the *I–V* and *C–V* characteristics have been compared. It has been seen that the barrier height value obtained from the *C–V* measurements are higher than that obtained from the *I–V* measurements at various temperatures. This behaviour has been attributed to the interfacial layer, the interface states and barrier inhomogeneity of the structure. Also this discrepancy can be due to the different nature of the *C–V* and *I–V* measurement techniques. A correlation seems to exist between the variation of the band gap and Fermi level energy of Si with temperature.
© 2005 Elsevier Ltd. All rights reserved.

Keywords: Capacitance; Schottky barrier; Polypyrrole

1. Introduction

Polymer electronics has attracted considerably interest in recent years with the discovery of conducting polymers. Thus, conducting polymers have recently received considerable attention owing to their numerous potential applications in electronic components such as Schottky diodes [1], field effect transistors (FETs) [2], batteries [3] etc. The efficiency of such devices depends on various factors such as preparation parameters and the stability of the polymer used. Polypyrrole (PPy) and its derivatives have been extensively investigated owing, among other properties, to the relatively high stability in ambient air [4].

The *C–V* measurements are one of the most popular electrical measurement techniques used to determine some important parameters of the Schottky diode, such as impurity concentrations, barrier heights (BHs) and Fermi energy levels [5,6]. There are different factors which effect the *C–V* measurements such as frequency and temperature. It is expected that the value of the capacitance increases with decreasing frequency and increasing temperature. It is very often observed experimentally that the Schottky barrier height calculated from the *I–V* characteristics does not equal the barrier height extracted from *C–V* measurements [7]. The *C–V* technique gives a convenient measure of the average Schottky barrier height (SBH) when the SBH is inhomogeneous. In the real Schottky diodes, the *I–V* characteristics usually deviate from the ideal thermionic emission difussion (TED) model, which assumes the junction to be abrupt with a fixed SBH. Recently, these deviations have been explained by assuming the presence of the barrier height inhomogeneities. The SBH is likely to be a function of the interface atomic structure, and the atomic inhomogeneities at the metal-semiconductor interface which are caused by grain boundaries, multiple phases,

* Corresponding author. Tel.: +90 442 231 4151; fax: +90 442 236 0948.
E-mail addresses: saydogan@atauni.edu.tr (Ş Aydoğan), saydogan43@yahoo.com (Ş Aydoğan).

0032-3861/$ - see front matter © 2005 Elsevier Ltd. All rights reserved.
doi:10.1016/j.polymer.2004.11.006

facets, defects, a mixture of different phases etc. The existence of small local regions ('patches') with different SBH was evidenced experimentally by using ballistic electron emission spectroscopy (BEES) [25–27]. In the model of Tung et al. [12], small regions or patches with a lower BH than the junction's main BH were assumed to exist at the junction. As mentioned in the model of Tung et al. [12] and Sullivan et al. [16], since the variation in SBH may occur even at a scale much smaller than the depletion region width, the interaction between patches should invariably lead to pinch-off of the conduction path of small low SBH regions that are surrounded by regions with high SBH. In such cases, the current across the MS contact may be greatly influenced by the presence of the SBH inhomogeneity [29]. Some studies [12,16,17,30] have shown that a variety of inhomogeneity models can be applied to describe the non-ideal SBD [28].

The capacitance signal comes from the modulation of the total space-charge as a function of bias. Generally, the capacitance measured for a Schottky diode is dependent on the reverse bias voltage and frequency. The voltage and frequency dependence is due to the particular features of a Schottky barrier, impurity level, high series resistance, interface states and interface layer between polymer and *n*-Si substrate, etc. At low frequency the capacitance measured is dominated by the depletion capacitance of the Schottky diode, which is bias-dependent and frequency-independent. As the frequency is increased, the total diode capacitance is affected not only by the depletion capacitance, but also the bulk resistance and dispersion capacitance, which is frequency-dependent and associated with hole emission from slowly responding deep impurity levels. Because of these effects, the capacitance dependence on bias becomes less pronounced or disappears. For an inhomogeneous SBH, the total space–charge is equal to that for a uniform SBH, with a height equal to the mathematical average of the inhomogeneous SBH [12]. This work presents the temperature and frequency effects on *C–V* measurements of Sn/PPy/*n*-Si contact and the discrepancy between barrier heights obtained from *I–V* and *C–V* measurements.

2. Experimental procedure

In this study, *n*-Si wafer with (100) orientation, 400 μm thickness and 1–10 Ω-cm resistivity was used and then, the *n*-Si wafer was chemically cleaned using the RCA cleaning procedure (i.e. 10 min boil in $NH_3+H_2O_2+6H_2O$ followed by a 10 min $HCl+H_2O_2+6H_2O$ at 60 °C) before making contacts. The ohmic contact was made by evaporating Au-Sb alloy on the back of the substrate, then was annealed at 420 °C for 3 min in N_2 atmosphere. The native oxide on the front surface of the *n*-Si substrate was removed in $HF+10H_2O$ solution. Finally, it was rinsed in de-ionised water for 30 s and was dried. After ohmic contact made, the ohmic contact side and the edges of the *n*-Si semiconductor substrate used as an anode were covered by wax so that the polished and cleaned front side of the sample (with a circle area, it has 1.7 mm diameter) was exposed to the electrolyte by mounting it in an experimental set-up employed for polymerization. A platinum plate was used as a cathode. The electrolyte was composed of 0.40 M pyrrole and 0.10 M tetrabutylammonium tetrafluoroborate. The pyrrole obtained from Fluka Chimika was used to prepare polypyrrole at room temperature. The electrolyte solution was prepared in a propylene carbonate solvent (Merck trademark). The polymer film was electrochemically deposited on surface of the sample under an electrolyte constant temperature of 45 °C and a constant current conditions of 4 mA. After polymerization process was carried out, the surface coated polypyrrole was cleaned by acetonitrile for 10 min at room temperature and was dried. Then to perform the electrical measurements Sn was evaporated on the polypyrrole at 10^{-5} torr. In this way the Sn/PPy/*n*-Si structure was obtained. A schematic csoss-section of the sample holder together with the Sn/PPy/*n*-Si structure is shown in Fig. 1. The *C–V* measurements of this structure were measured with an HP4192A LF capacitancemeter at 10, 50, 500, 1000 kHz frequencies and the *I–V* measurements were performed with KEITLEY 487 Picoammeter/Voltage Source, a temperature range of 77–300 K by using a homemade liquid nitrogen cryostat equipped with a temperature controller in darkness.

3. Results and discussion

Differential capacitance measurements on a Schottky barrier measure the response of the barrier to an a.c. voltage superposed on a d.c. voltage. When the d.c. voltage corresponds to a reverse bias, the differential capacitance represents the response of the depletion layer to the a.c. signal. It is convenient to examine *C–V* data for Schottky diodes by plotting C^{-2}–*V* for reverse bias. In metal/semiconductor contacts the depletion layer capacitance is given as follows [8],

$$C^{-2} = \frac{2(V_d + V)}{\varepsilon_s \varepsilon_0 q A^2 N_d} \quad (1)$$

where V_d is the diffusion potential at zero bias which is determined from the extrapolation of the linear $1/C^2$–*V* plot to the *V* axis, *A* is the effective area of the diode and ε_s is the

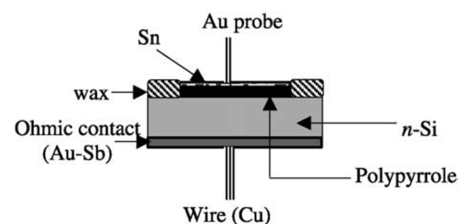

Fig. 1. Cross-section of the sample holder and PPy/*n*-Si structure.

dielectric constant of the semiconductor (=11.7 for Si) [9], ε_0 is the dielectric constant of vacuum ($=8.85\times10^{-14}$ F/m) and N_d is the concentration of ionized donors.

The value of the barrier height by *I–V* characteristics is obtained by;

$$q\Phi_b = kT\ \ln(AA^*T^2/I_0) \tag{2}$$

where Φ_b is the zero-bias barrier height (BH), q the electron charge, k the Boltzmann's constant, T the temperature in Kelvin, A^* the effective Richardson constant and is equal to 112 A/cm^{2}K^2 for *n*-type Si and I_0 is the saturation current.

The value of the barrier height Φ_b can be calculated by the following well-known equation, using *C–V* measurements,

$$\phi_b = V_d + V_n \tag{3}$$

where V_n is the potential difference between the Fermi energy level (E_f) and the bottom of the conduction band in the neutral region of *n*-Si, which is directly equal to E_f, and can be calculated by knowing N_d and N_c, density of states in the conduction band, which is $N_c=2.8\times10^{19}$ cm^{-3} for Si at room temperature [25];

$$N_d = N_c\ \exp(V_n/kT) \tag{4}$$

Eq. (3) is valid for only the diodes which show ideal behavior. For the ideal contacts, the ideality factor (n) is equal to unit, otherwise it is higher than unit. In an ideal Schottky barrier, the barrier height is independent of the bias and current flows only due to thermionic emission $n=1$. Factors which make n larger than unity are the bias dependence of barrier height, electron tunneling through the barrier, and the carrier recombination within the depletion region. Since these devices operate under high-level injection, deviations from the ideal behavior are also observed because of enhanced minority carrier transport by the drift field in the quasineutral region. For nonideal structures, this equation should be corrected by taking into account of ideality factor [18]:

$$\phi_b = c_2V_d + V_n \tag{5}$$

where c_2 corresponds to $1/n$. Where, the values of the ideality factor (n) have been obtained from the forward bias *I–V* characteristics.

Measurement of the depletion region capacitance under forward bias is difficult because the diode is conducting and the capacitance is shunted by a large conductance. However, the capacitance can be easily measured as a function of the reverse bias [10]. Figs. 2, 4, 6 and 8 show the reverse bias *C–V* characteristics, Figs.3, 5, 7 and 9, show the reverse bias C^{-2}–*V* characteristics of the Sn/PPy/*n*-Si structure at 10, 50, 500, 1000 kHz frequencies respectively, in the range of 77–300 K. In these figures, it can be seen that at low frequencies and at high temperatures the values of capacitance are shown to increase. This observation may be attributed to the capacitive response of interface states to the measurement

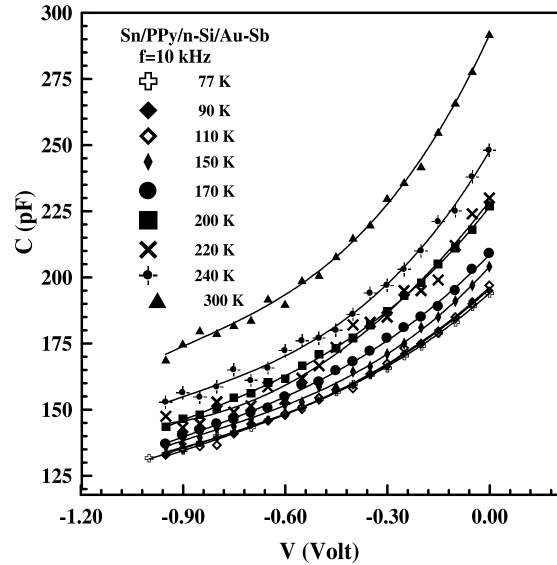

Fig. 2. The reverse bias *C–V* characteristics of the PPy/*n*-Si structure at $f=$ 10 kHz and in the range of 77–300 K.

frequency. In general, at sufficiently high frequencies ($f\geqq500$ kHz) the interface states do not contribute to the capacitance [13–15]. When the frequencies increase, the values of the diffusion potential do increase too. This case may be due to interface trapped charge, which were not taken into account for the extraction of the depletion region width from *C–V* characteristics.

Also, it can be seen from the reverse bias C^{-2}–*V* figures that these curves are linear, both at low and high frequencies. This indicates that the formation of these structure is resemble a Schottky diode and allows the use of the simple depletion layer theory (Eq. (1)) [11]. But at the forward bias, irregularities occur [19,20]. The non-linearities express themselves as excess capacitance or, on the other hand as

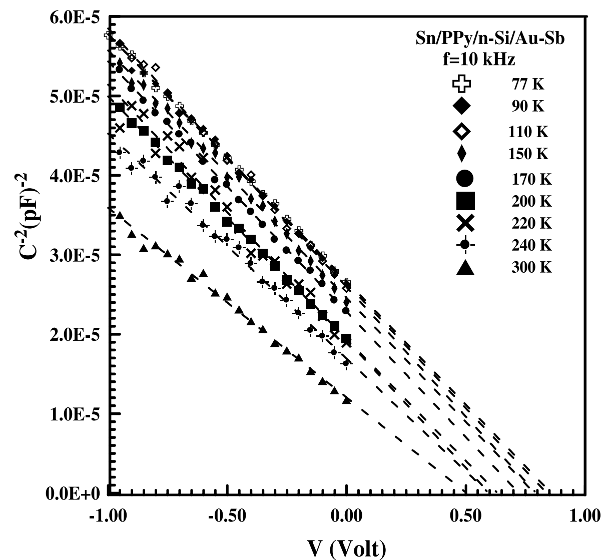

Fig. 3. The reverse-bias C^{-2}–*V* characteristics of the PPy/*n*-Si structure at $f=10$ kHz and in the range of 77–300 K.

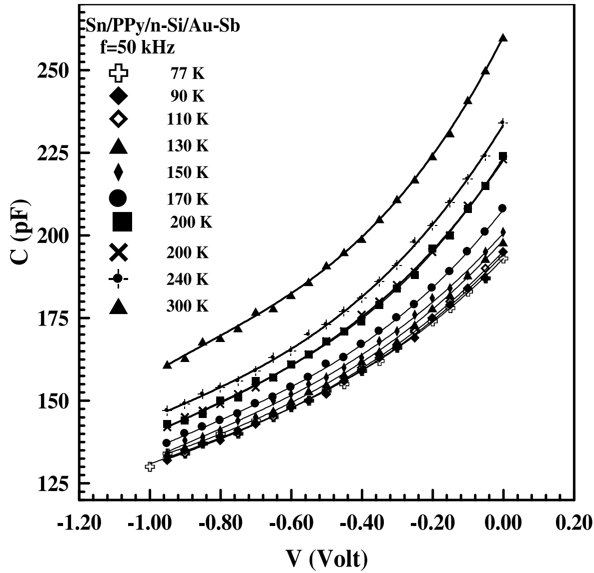

Fig. 4. The reverse bias C–V characteristics of the PPy/n-Si structure at $f=$ 50 kHz and in the range of 77–300 K.

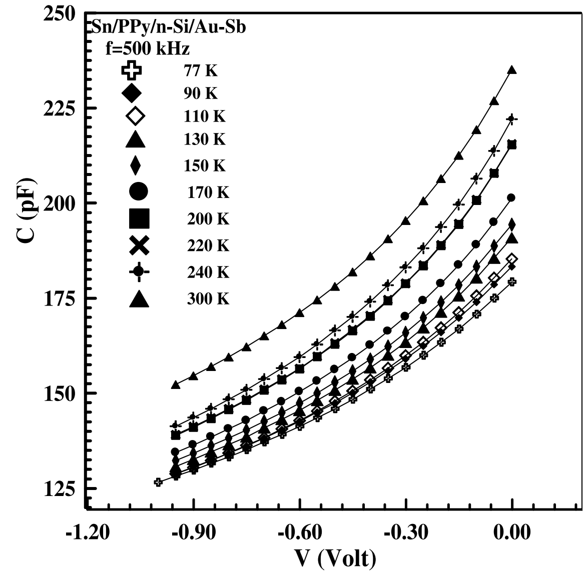

Fig. 6. The reverse bias C–V characteristics of the PPy/n-Si structure at $f=$ 500 kHz and in the range of 77–300 K.

inductive reactance. These phenomena were currently not fully understood and were attributed to interface states [21–23].

Fig. 10 presents the barrier height against temperature, obtained from the I–V (apparent BH) characteristics using Eq. (2) and from the C–V measurements. The barrier height extracted from the C–V measurements increase slowly with decreasing temperature, in contrast to the I–V measurements. Therefore, there is more current at low temperature than predicted by thermionic emission theory and the results of the C–V measurements. Also, the values of the barrier height extracted from the C–V curves are higher than derived from the I–V measurements as expected. Although, this discrepancy could be explained by the existence of excess capacitance at the structure due to the an interfacial layer or trap states in the semiconductor, the existence of the barrier inhomogeneity offers another explanation [16,17]. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise, they will yield different values.

Fig. 11 shows the variation of band gap and Fermi energy level of the structure as a function of temperature at 1 MHz frequency. The similar characteristics were obtained from the other frequencies as well. The C–V BHs are also associated with the temperature dependence of the valance band edge position at the surface. The reason of the

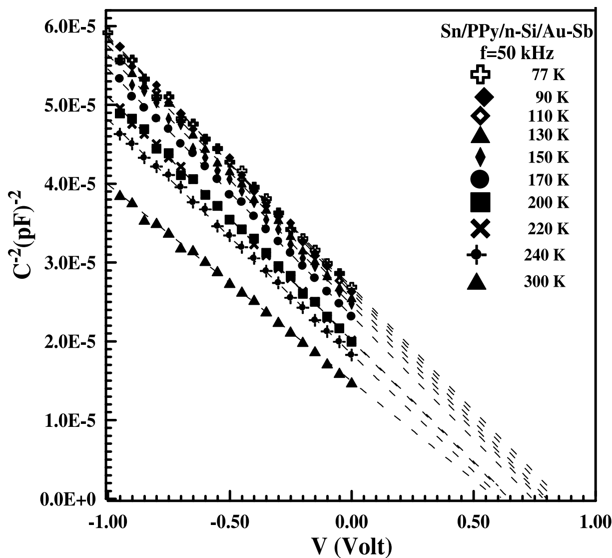

Fig. 5. The reverse-bias C^{-2}–V characteristics of the PPy/n-Si structure at $f=50$ kHz and in the range of 77–300 K.

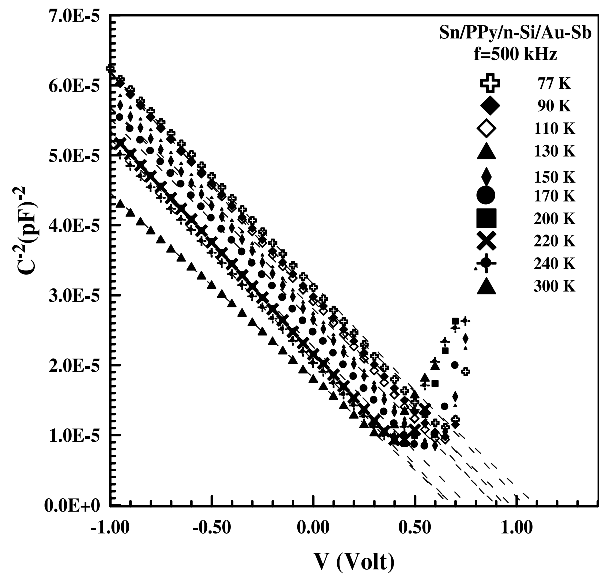

Fig. 7. The reverse-bias C^{-2}–V characteristics of the PPy/n-Si structure at $f=500$ kHz and in the range of 77–300 K.

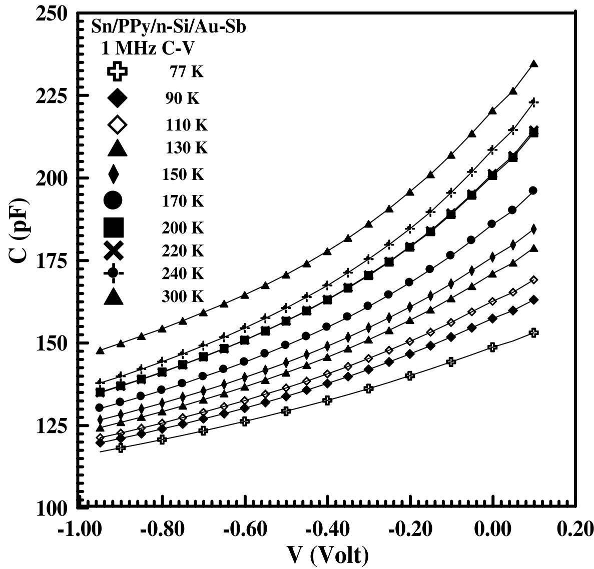

Fig. 8. The reverse bias C–V characteristics of the PPy/n-Si structure at $f=$ 1000 kHz and in the range of 77–300 K.

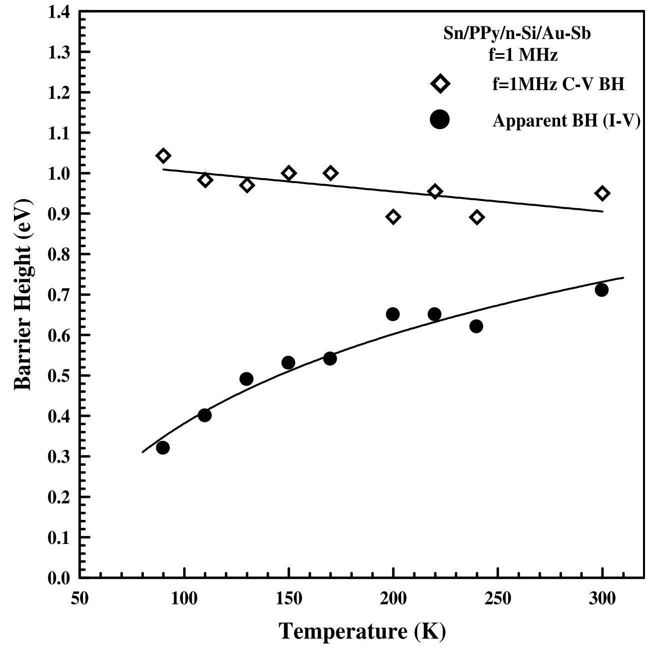

Fig. 10. Temperature dependence of the barrier heights obtained from I–V and C–V measurements for PPy/n-Si structure in the range of 77–300 K. Solid lines correspond to the fits to the related barrier heights curves.

difference in temperature coefficients is possibly the extremely high values of n at low temperatures, which this provides an additional evidence to believe that the patchiness of the contact area increases towards low temperatures and thus, the diode exhibits a nonideal behavior [24]. The band gap, and thus the conduction and valance band edges of Si do shift slightly with temperature. The linear fitting of E_f and E_g yields the values of $E_f(T=0)=0.02$ eV and, $E_g(T=0)=1.18$ eV in the temperature range 77–300 K and the temperature coefficient, of the band gap of PPy/n-Si has been found a value of 1.8×10^{-4}. Obviously, the relationship is linear and controversial. Hence, a correlation seems to exist between the variation of the band gap and Fermi level energy of Si with temperature. This behavior requires that the ionized donor concentration, N_d should increase at high temperatures as E_f increases and E_g decreases linearly.

In conclusion, temperature dependence of the I–V characteristics and temperature and frequency dependence of reverse bias C–V characteristics of PPy/n-Si structure were investigated. It was seen that there is a discrepancy between apparent barrier heights (BHs) obtained from I–V and C–V measurements. This discrepancy was especially

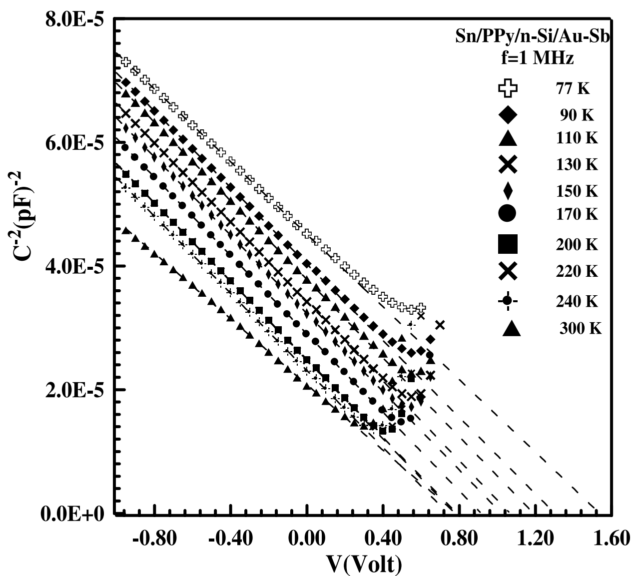

Fig. 9. The reverse-bias C^{-2}–V characteristics of the PPy/n-Si structure at $f=1000$ kHz and in the range of 77–300 K.

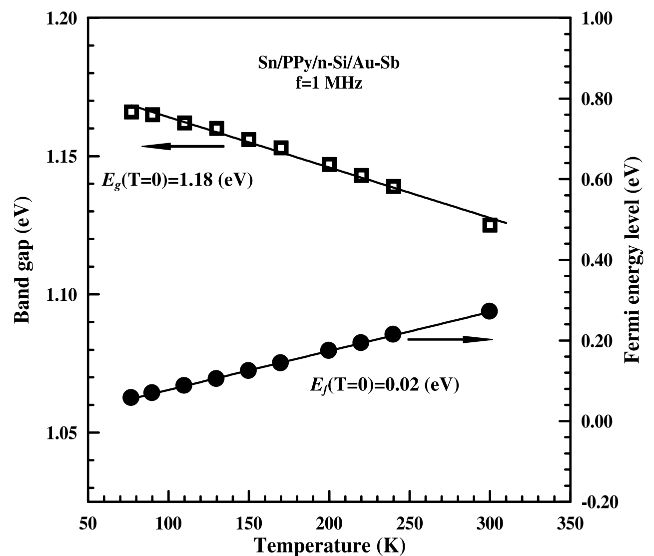

Fig. 11. Temperature dependence of band gap and Fermi energy level of PPy/n-Si structure at $f=1000$ kHz, in the range of 77–300 K.

explained by introducing a spatial distribution of SBHs due to barrier height inhomogeneities that occur at the PPy/*n*-Si interface. Also, as expected, at low frequencies and at high temperatures the values of capacitance are shown to increase. This situation was attributed to the capacitive response of interface states to the measurement frequency.

References

[1] Glenis S, Horowitz G, Tourillon G, Garnier F. Thin Solid Films 1984; 111:93.
[2] Tsuma A, Koezuka H, Ando T. Appl Phys Lett 1986;49:1210.
[3] Onganer Y, Sağlam M, Türüt A, Efeoğlu H, Tüzemen S. Solid State Electron 1996;39:677.
[4] Erlandsson R, Inganäs O, Lundström I, Salaneck WR. Synth Met 1985;10:303.
[5] Chattopadhyay P, Ray-Chaudhuri B. Solid State Electron 1993;36: 605.
[6] Zohta Y. Solid State Electron 1973;16:1029.
[7] Osvald J, Burian E. Solid-State Electron 1998;42:191.
[8] Ziel AV. Solid state physical electron, 2nd ed. NJ: Prentice-Hall: Englewood Cliffs; 1968.
[9] Neamen DA. In: Semiconductor physics and devices; basic principles, 1992. p. 144.
[10] Sharma BL. In: Metal-semiconductor Schottky barrier junctions and their applications. New York: Plenum; 1984. p. 31.
[11] Sze SM. Physics of the semiconductor devices. New York: Wiley; 1981.
[12] Tung RT. Mater Sci Eng 2001;R35:1–138.
[13] Türüt A, Yalçın N, Sağlam M. Solid-State Electron 1992;35:835.
[14] Özdemir S, Altındal Ş. Solar Energy Mater Solar Cells 1994;32:115.
[15] Fonash SF. J Appl Phys 1983;56:1966.
[16] Sullivan JP, Tung RT, Pinto MR, Graham WR. J Appl Phys 1991; 70(12):7403.
[17] Werner JH, Gütter HH. J Appl Phys 1991;69(3):1522.
[18] Türüt A, Sağlam M, Efeoğlu H, Yalçın N, Yıldırım M, Abay B. Physica B 1995;205:41.
[19] Champness CH, Clark WR. Appl Phys Lett 1990;56:1104.
[20] Liou JJ, Malocha DC. J Appl Phys 1989;65:1782.
[21] Osvald J, Burian E. Solid-State Electron 1998;42:191.
[22] Wu X, Yang ES. J Appl Phys 1990;65:3560.
[23] Wu X, Yang ES, Evans HI. J Appl Phys 1990;68:2845.
[24] Coşkun C, Aydoğan Ş, Efeoğlu H. Semicond Sci Tech 2004;19(2): 242–6.
[25] Hecht MH, Bell LD, Kaiser WJ, Grunthaner FJ. Appl Phys Lett 1980; 55:780.
[26] Formen S, Van Meirhaeghe RL, de Vrieze A, Strubbe K, Gomes WP. Semicond Sci Technol 2001;16:975.
[27] Detavernier C, Van Meirhaeghe RL, Donaton R, Maex K, Cardon F. J Appl Phys 1998;84:3226.
[28] Nuhoğlu Ç, Aydoğan Ş. A Türüt. Semicond Sci Technol 2003;18: 642–6.
[29] Song YP, Van Meirhaeghe RL, Lafl'ere WH, Cardon F. Solid-State Electron 1986;29:633.
[30] Dobrocka E, Osvald J. Appl Phys Lett 1994;65:575.